Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A synchronous transport module (STM) comprising:

a UTOPIA interface chip for transmitting a UTOPIA level 2 data;

one pair of STM interface chips for receiving a UTOPIA level 1 data;

a UTOPIA memory for converting the UTOPIA level 2 data into the UTOPIA level 1 data, and transferring the UTOPIA level 1 data to one of the pair of the STM interface chips according to a transmission address; and,

a UTOPIA interface control part for converting the transmission address depending on states of the STM interface chips, the UTOPIA interface control part including bits which are used for determining whether the STM interface chips are to be in duplex states and/or simplex states, and other bits which are used for determining whether the respective STM interface chips are to be in active states and/or standby states in the duplexing.

2. (Original) A synchronous transport module as claimed in claim 1, wherein the UTOPIA memory is an FIFO memory.

3. (Original) A synchronous transport module as claimed in claim 1, wherein the UTOPIA interface control part converts the transmission address by putting the chip in a failed state into a standby state and the chip in a regular state into an active state.

4. (Original) A synchronous transport module as claimed in claim 3, wherein the conversion of the transmission address is inversion of a state of a least significant bit of the bits in the transmission address.

5. (Currently amended) An synchronous transport module (STM) comprising:

a UTOPIA interface chip for transmitting/receiving a UTOPIA level 2 data;

one pair of STM interface chips for receiving/transmitting a UTOPIA level 1 data;

a UTOPIA memory for converting the UTOPIA level 2 data into the UTOPIA level 1 data, and transferring the UTOPIA level 1 data to one of the pair of the STM interface chips according to a transmission address;

a first bus matching memory for converting the UTOPIA level 1 data from a first STM interface chip of the pair of the STM interface chips into the UTOPIA level 2 data, and transferring the converted UTOPIA level 2 data to the UTOPIA interface chip according to a reception address;

a second bus matching memory for converting the UTOPIA level 1 data from a second STM interface chip of the pair of the STM interface chips into the UTOPIA level 2 data, and transferring the converted UTOPIA level 2 data to the UTOPIA interface chip according to the reception address;

a processor for reading states of the STM interface chips; and,

a UTOPIA interface control part for converting the transmission address and the reception address under the control of the processor, the UTOPIA interface control part including bits which are used for determining whether the STM interface chips are to be in duplex states and/or simplex states, and other bits which are used for determining whether the respective STM interface chips are to be in active states and/or standby states in the duplexing.

6. (Original) An STM as claimed in claim 5, wherein the UTOPIA interface control part converts the transmission address and the reception address by putting the chip in a failed state into a standby state and the chip in a regular state into an active state.

7. (Original) An STM as claimed in claim 5, wherein the processor is a programmable logic device (PLD).

8. (Original) An STM as claimed in claim 5, wherein the UTOPIA memory, the first bus matching memory, and the second bus matching memory are first in first out (FIFO) memories.

9. (Canceled)

10. (Currently amended) A method for transmitting a data in an STM including a UTOPIA interface chip for transmitting a UTOPIA level 2 data having a transmission data, one pair of STM interface chips for receiving a UTOPIA level 1 data, a UTOPIA memory for converting the UTOPIA level 2 data into the UTOPIA level 1 data, and transferring the UTOPIA level 1 data to one of the pair of the STM interface chips according to the transmission address, and a processor, the method comprising ~~the steps of~~:

(a) checking fail states of the STM interface chips through the processor,

(b) converting the transmission address by putting the chips in failed states to standby states, and the chips in regular states to active states, among the STM interface chips, ~~and~~

(c) assigning each of the STM interface chips to operate in a duplex mode or a simplex mode, for the respective communication mode, and

(d) assigning each of the STM interface chips the operational state of active state or

standby state, based on an operational status of the respective STM interface chip

~~(c) transmitting~~(e) transmitting the converted UTOPIA level 1 data to the chips in the active state among the STM interface chips according to the transmission address.

11. (Original) A method as claimed in claim 10, wherein the processor is a programmable logic device (PLD).

12. (Original) A method as claimed in claim 10, wherein the conversion of the transmission address is inversion of a state of a least significant bit of the bits in the transmission address.

13. (Currently amended) A synchronous transport module (STM), comprising:

a plurality of STM interfaces that communicate universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) level-1 data;

a UTOPIA interface control part that communicates UTOPIA level-2 data and assigns an operational state and a communication mode to each of the plurality of STM interfaces; and

a plurality of bus-matching first in first out (FIFO) memories that communicate the UTOPIA level-1 data with the plurality of STM interfaces and the UTOPIA level-2 data with

the UTOPIA interface control part, convert the UTOPIA level-1 data to the UTOPIA level-2 data, and convert the UTOPIA level-2 data to the UTOPIA level-1 data, wherein

each of the plurality of bus-matching FIFO memories corresponds to a separate one of the plurality of STM interfaces and communicates UTOPIA level-1 data with only the corresponding STM ~~interface~~interface,

wherein the UTOPIA interface control part assigns each of the plurality of STM interfaces to operate in a duplex mode or a simplex mode, for the respective communication mode, and assigns each of the plurality of STM interfaces the operational state of active state or standby state, based on an operational status of the respective STM interface.

14. (Canceled)

15. (Currently amended) The STM of ~~claim 14~~claim 13, wherein:

each of the STM interfaces assigned the duplex mode of operation is paired with another STM interface and only one STM interface of each pair is assigned the active state; and

only the active state STM interface, of each pair of STM interfaces, communicates with the UTOPIA interface control part.

16. (Currently amended) The STM of ~~claim 14~~claim 13, wherein each of the plurality of STM interfaces experiencing a detectable fault is assigned the standby state.

17. (Original) The STM of claim 15, wherein the UTOPIA interface control part changes a portion of a destination address of the UTOPIA level-2 data to uniquely identify the one STM interface, of a particular pair of duplex mode STM interfaces that are both partially addressed by the destination address, that is currently assigned the active state.

18. (Currently amended) A synchronous transport module (STM) communication method, comprising:

communicating universal test, operation, and physical interface for asynchronous transport mode (UTOPIA) level-1 data between a plurality of STM interfaces and a plurality of bus-matching first in first out (FIFO) memories;

communicating UTOPIA level-2 data between a UTOPIA interface control part and the plurality of bus-matching FIFO memories; ~~and~~

converting the UTOPIA level-1 data, received by the plurality of bus-matching FIFO memories, to the UTOPIA level-2 data and converting the UTOPIA level-2 data, received by the plurality of bus-matching FIFO memories, to the UTOPIA level-1 ~~data,~~data;

assigning each of the plurality of STM interfaces to operate in a duplex mode or a simplex mode of communication; and

assigning each of the plurality of STM interfaces an operational state of active state or standby state, based on an operational status of the respective STM interface,

wherein each of the plurality of bus-matching FIFO memories corresponds to a separate one of the plurality of STM interfaces and communicates UTOPIA level-1 data with only the corresponding STM interface.

19. (Canceled)

20. (Currently amended) The method of ~~claim 19~~claim 18, further comprising:

pairing each of the STM interfaces assigned the duplex mode of operation with another STM interface, wherein

only one STM interface of each pair is assigned the active state, and

only the active state STM interface, of each pair of STM interfaces, communicates with the UTOPIA interface control part.

21. (Currently amended) The method of ~~claim 19~~claim 18, further comprising assigning each of the plurality of STM interfaces experiencing a detectable fault ~~the~~ to the standby state.

22. (Original) The method of claim 20, further comprising changing a portion of a destination address of the UTOPIA level-2 data to uniquely identify the one STM interface, of a particular pair of duplex mode STM interfaces that are both partially addressed by the destination address, that is currently assigned the active state.